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Description

Memory cell and method for fabricating a memory device

5   The invention relates to a method for fabricating a
     memory device, which includes semiconductor structures,
     with memory cells, in which digital information is
     stored in a storage layer, in which method:
     -    two source/drain regions, which are spaced apart
10   from one another by a channel region, are formed
          in a semiconductor substrate,
     -    a gate dielectric is provided on a substrate
          surface of the semiconductor substrate,
          substantially above the channel region.
15
     Moreover, the invention relates to a memory cell having
     a storage layer which stores a digital information
     item, having two source/drain regions, which are formed
     in a semiconductor substrate and are spaced apart from
20   one another by a channel region, and a gate dielectric,
     which is provided on a substrate surface of the
     semiconductor substrate, substantially above the
     channel region.

25   Memory cells, in which digital information is stored as
     a charge state of a charge-storing unit, are used to
     fabricate DRAM (dynamic random access memory) or EEPROM
     (electrically erasable and programmable read-only
     memory) memory devices. To enable the charge state of
30   the charge-storing unit in the memory cell to be
     reliably measured, the quantity of stored charge must
     not drop below a predetermined minimum. This fact
     entails considerable outlay when further reducing the
     size of the memory cells, since the smaller the memory
35   cell becomes, so too the lower the possible quantity of
     stored charge will be and the more complex it will be
     to reliably detect the charge state of the cell.

One approach aimed at improving the situation consists in designing the charge-storing unit of a memory cell, which is usually designed as a capacitor connected to a
5   select transistor, as a storage layer which stores charge and is arranged above the channel region of a field-effect transistor. As a result, the charge stored in the storage layer can be capacitively introduced into the channel region of the field-effect transistor,
10   thereby utilizing an amplification of the field-effect transistor. On account of the amplification of the field-effect transistor, just a small quantity of stored charge is sufficient to allow reliable detection of the stored information. This approach is used, for
15   example, for ferroelectric field-effect transistors, in which the storage layer consists of a ferroelectric material. A detailed description of a field-effect transistor with ferroelectric storage layer is to be found in the publication by I. Ishiwara, Recent
20   Progress of FET-Type Ferroelectric Memories, Integrated Ferroelectrics 34 (2001), 11-20.

If the storage layer consists of an organic material, it is customary for the organic storage layer, on
25   account of the small quantity of stored charge, in accordance with the approach described above to be arranged directly above the channel region of a field-effect transistor, so that the amplification of the field-effect transistor can be utilized. The
30   organic storage layer may consist, for example, of porphyrin molecules. Oxidation and reduction of the porphyrin molecules lead to different charge states in the storage layer. A reduction corresponds to the storage layer being charged with electrons, and an
35   oxidation corresponds to the storage layer being discharged. To determine the charging state of the

storage layer, which represents the digital information, a constant read voltage is applied to a gate electrode of the field-effect transistor, and a resulting drain current between the two source/drain
5 regions is detected. If the storage layer is charged with electrons, a threshold voltage, above which the drain current is approximately exponentially dependent on the level of the gate voltage, shifts toward higher voltage values. If a suitable read voltage is used, the
10 drain current is approximately nonexistent in the reduced state of the storage layer and characterizes a logic state of zero. In the oxidized state of the storage layer, a drain current flows and characterizes a logic state one.
15
A conventional field-effect transistor of a memory cell with an organic storage layer is illustrated in Figure 1. Two source/drain regions 5 are separated from one another by a channel region 4 in a semiconductor
20 substrate. On the channel region 4 there is a gate dielectric 6, and on the gate dielectric 6 there is an organic storage layer 10. A gate electrode 7 is provided on the organic storage layer 10.

25 A predetermined read voltage is applied to the gate electrode 7, and when this read voltage is applied, a drain current or virtually no drain current flows between the two source/drain regions 5 depending on whether the storage layer 10 is in a reduced state or
30 an oxidized state.

The way in which the drain current is dependent on the charge state of the storage layer as described is illustrated in Figure 5. The logarithm of the drain
35 current is plotted on the ordinate, and the gate voltage of an n-channel field-effect transistor,

containing an organic storage layer, of a memory cell
as illustrated in Figure 1 is plotted on the abscissa.
A memory cell of this type can also be implemented
without restriction using a p-channel field-effect
5   transistor. The current/voltage characteristic curve
indicated by a corresponds to the field-effect
transistor with a discharged, oxidized storage layer.
The current/voltage characteristic curve denoted by b
corresponds to the field-effect transistor with a
10   charged, reduced storage layer. Oxidization or
reduction of the organic layer leads to a parallel
shift in the current/voltage characteristic curve of
the field-effect transistor along the abscissa. The
value U_L marked on the abscissa indicates the level of
15   the read voltage at the gate electrode. If the storage
layer of the field-effect transistor is in a reduced
state with the current/voltage characteristic curve b,
the drain current D_2 on the ordinate associated with the
value UL is virtually zero. If the storage layer is in
20   oxidized state with the current/voltage characteristic
curve a, the drain current D1 associated with the value
UL adopts a significantly higher value. It is therefore
possible to distinguish between two charge states of
the storage layer with a constant read voltage at the
25   gate electrode, on the basis of the level of the
resulting drain current.

However, there are disadvantages associated with the
fabrication of memory devices having the memory cells
30   illustrated in Figure 1. In a conventional method for
fabricating memory devices, semiconductor structures of
the field-effect transistors of memory cells and their
insulation with respect to one another are processed
first of all. This concludes a part of the overall
35   process which is also referred to as the FEOL (front
end of line) and involves the processing of

monocrystalline   and   polycrystalline   semiconductor
structures. Processing of the semiconductor structures
is followed by contact-making and connection of the
individual   monocrystalline   and   polycrystalline
5   semiconductor structures. This part of the overall
process is also known as the BEOL (back end of line).
Since very high temperatures of up to 1100 degrees
Celsius are used in the FEOL, the conventional memory
cell with field-effect transistor with an organic
10   storage layer which is arranged on the gate dielectric
beneath   the   polycrystalline   gate   electrode   as
illustrated in Figure 1 is very difficult to implement,
since in most cases, organic storage layers are very
temperature-sensitive, and arranging them beneath the
15   gate electrode requires the storage layer to be applied
in the FEOL section, in which the storage layer is
exposed to very high temperatures.

However, if extremely thin insulator layers are used,
20   organic   storage   layers   have   the   advantage   over
inorganic storage layers of permanent charge storage.
Moreover,   organic   storage   layers   have   good
scaleability. This is advantageous for further
reduction of the size of memory cells.
25
Therefore, the invention is based on the object of
providing a method for fabricating a memory device with
memory cells in which digital information is stored in
a temperature-sensitive storage layer. The invention is
30   also based on the object of providing a memory cell
having a temperature-sensitive storage layer.

In a method of the type described in the introduction,
this object is achieved by the features listed in the
35   characterizing clause of patent claim 1. The object is
achieved by memory cells as claimed in patent claim 11.

Advantageous refinements of the invention will emerge
from the respective subclaims.

The invention provides a method for fabricating a
5   memory device, which includes semiconductor structures,
with memory cells in which digital information is
stored in a storage layer. In the method, two
source/drain regions, which are spaced apart from one
another by a channel region, are formed in a
10   semiconductor substrate. A gate dielectric is provided
on a substrate surface of the semiconductor substrate,
substantially above the channel region. According to
the invention, a first gate electrode is arranged on
the gate dielectric. Processing of the semiconductor
15   structures is concluded before the storage layer is
applied. A conductive connection is provided between
the storage layer and the first gate electrode. An
insulator layer is provided above the storage layer,
and a second gate electrode is provided on the
20   insulator layer.

In the method according to the invention, the
processing of polycrystalline and monocrystalline
semiconductor structures, in which high temperatures
25   are employed, is concluded prior to the application of
the storage layer. Examples of polycrystalline or
monocrystalline semiconductor structures include
source/drain regions, channel region and first gate
electrode of a field-effect transistor. Therefore, the
30   application of the storage layer is shifted into a part
of the processing in which contact-making and
connecting of the individual monocrystalline and
polycrystalline semiconductor structures takes place
and in which high temperatures are no longer employed.
35   Shifting the application of the storage layer into a
later part of the processing generally also requires

the storage layer to be separated from the first gate electrode, which is generally formed from a polycrystalline semiconductor substrate. Therefore, a conductive connection is provided between the storage layer and the first gate electrode, for example in the form of a metal-filled contact hole which is introduced into an insulation layer. The second gate electrode, which is separated by an insulator layer from the storage layer, which is conductively connected to the first gate electrode of the field-effect transistor, is used to drive the field-effect transistor.

The main advantage of the method according to the invention consists in the fact that the thermal stressing of the storage layer is significantly reduced in a simple way and without the need for additional process steps by shifting the application of the storage layer into a later part of the processing. This considerably widens the range of materials which are envisaged for storage layers. The method according to the invention makes it possible to use even organic storage layers.

It is advantageous for the storage layer to be arranged between a first and a second electrode. As a result of additionally formed electrodes being provided, it is possible to use electrode materials which are suitably adapted to a material of the storage layer. A further advantage is that the electrode surfaces can be selected independently of the transistor and contact surfaces.

It is preferable for the first electrode to be formed by a portion of the conductive connection. If the conductive connection is formed, for example, as a contact hole filled with a conductive material, it is

also possible for the storage layer to be applied direct to the contact hole filling. This allows one process step to be saved.

5   It is advantageous for one of the metals aluminum, tungsten or copper to be provided for the first and second electrodes. These are metals which are also used in the other process steps. Therefore, forming the electrodes would not require an additional process
10 step.

It is preferable for one of the precious metals platinum, gold or silver to be provided for the first and second electrodes.

15

It is preferable for the first electrode to be formed in a first metal level and the second electrode to be formed in a second metal level. The conductive connection between the first gate electrode and the
20 first electrode is produced by a contact hole filled with conductive material.

Forming the first and second electrodes in respective metal levels advantageously means that there is no need
25 for an additional process step for forming the electrodes, since the electrodes can be processed together with interconnects which are formed in the metal levels. An additional advantage of this procedure is that the storage layer can easily be introduced into
30 a hole which is provided in an insulation layer which electrically separates the two metal levels from one another. The conductive connection between the first gate electrode and the first electrode is produced by a contact hole filled with conductive material. There is
35 a further insulation layer between the first metal level and the first gate electrode. Contact holes are

introduced into this insulation layer to produce
conductive connections to the first metal level. There
is advantageously no need for an additional process
step to produce the contact hole for the conductive
5   connection between the first gate electrode and the
first electrode.

It is advantageous for the first and second electrodes
each to be formed in a metal level which is in each
10 case processed later in the process sequence. The
conductive connection between the first electrode and
the first gate electrode is produced by contact holes
arranged above one another and filled with conductive
material. The advantage of this procedure is that as a
15 result of the electrodes being formed at a point in
time which comes later in the overall process sequence,
i.e. as a result of the first and second electrodes
being shifted to higher metal levels, the thermal
stressing to which the storage layer is exposed is
20 reduced further. The conductive connection between the
first gate electrode and the first electrode is
advantageously produced by contact holes which are
arranged above one another and are introduced into the
insulation layers between the metal levels. The contact
25 holes which are arranged above one another and are
filled with conductive material produce a conductive
connection through a plurality of metal levels.

It is preferable for the storage layer provided to be
30 an organic layer which may be provided, for example,
having porphyrin molecules. Organic storage layers,
such as for example those which consist of porphyrin
molecules, have the advantage of permanent charge
storage and low leakage currents. The gate dielectric,
35 through which the charge carriers can flow out, can be
made thinner than if inorganic storage layers are used.

A thinner gate dielectric offers the advantage of
accelerated charging and discharging of the storage
layer and therefore faster access times. Moreover,
organic storage layers have the advantage of good
5   scaleability. This is beneficial for a further
reduction in the size of memory cells.

Advantageously, to produce source and drain lines, the
source/drain regions of memory cells arranged in rows
10   which are respectively adjacent within a row are
electrically conductively connected to one another by
doped regions provided in the semiconductor substrate.
After a predetermined number of source/drain regions
which have been electrically conductively connected to
15   one another by doped regions in the semiconductor
substrate, conductive connections to interconnects,
which are formed in a metal level and connect the
source/drain regions of memory cells, are provided. The
doped regions can be introduced into the semiconductor
20   substrate by a dopant diffusing in. The advantage is
that it is possible to avoid an increase in the surface
area taken up by the memory cell on a semiconductor
wafer. Maintaining minimum distances between contacts
to the metal level and electrodes, between which the
25   storage layer is arranged, would lead to an increase in
the surface area taken up by the memory cell. The
provision of lines which are formed as doped regions in
the semiconductor substrate advantageously allows
contacts to the metal level to be provided after a
30   predetermined number of memory cells, and consequently
there is no longer any need to provide a contact to the
metal level in each memory cell.

A memory cell is provided having a storage layer, which
35   stores a digital information item, having two
source/drain regions, which are formed in a

semiconductor substrate and are spaced apart from one
another by a channel region, and having a gate
dielectric which is arranged on a substrate surface of
the semiconductor substrate, substantially above the
5   channel region. According to the invention, a first
gate electrode is arranged on the gate dielectric. The
storage layer is arranged on the first gate electrode
or at a distance from the first gate electrode. There
is a conductive connection between the storage layer
10 and the first gate electrode. An insulator layer is
provided above the storage layer, and a second gate
electrode is provided on the insulator layer.

The memory cell according to the invention has the
15 advantage that monocrystalline and polycrystalline
semiconductor structures, such as for example channel
region, source/drain region and first gate electrode of
a field-effect transistor, can be processed prior to
the application of the storage layer. Since high
20 temperatures are usually employed during the processing
of semiconductor structures, the application of the
storage layer at a later time reduces the thermal
stressing of the storage layer. This prevents
degradation of, for example, organic storage layers.
25 The storage layer is charged and discharged as a result
of the conductive connection of the storage layer to
the first gate electrode. The memory cell according to
the invention allows the range of materials which can
be used to form the storage layers to be widened
30 considerably.

The storage layer is arranged between a first and a
second electrode. The provision of additionally formed
electrodes makes it possible to use electrode materials
35 which are suitably adapted to a material of the storage
layer. Another advantage is that the electrode surfaces

can be selected independently of the transistor and contact surfaces.

It is preferable for the first electrode to be formed
5   by a portion of the conductive connection. For example, if the conductive connection is designed as a contact hole filled with a conductive material, it is also possible for the storage layer to be applied direct to the contact hole filling, allowing one process step to
10 be saved.

The first and second electrodes advantageously consist of one of the metals aluminum, tungsten or copper. These are metals which are also used in the other
15 process steps. Therefore, forming the electrodes would not require an additional process step.

It is preferable for the first and second electrodes to consist of one of the precious metals platinum, gold or
20 silver.

It is preferable for the first electrode to be formed in a first metal level and the second electrode to be formed in a second metal level. The conductive
25 connection between the first gate electrode and the first electrode is provided by a contact hole filled with conductive material. Forming the electrodes, between which the storage layer is arranged, in adjacent metal levels containing interconnects and
30 contact holes has the advantage that additional process steps for forming the electrodes are avoided. If the conductive connection is produced by a contact hole which is filled with conductive material and has been introduced into an insulation layer arranged between
35 the first gate electrode and the first metal level,

there is advantageously no need for any additional
process steps.

The first and second electrodes are each formed in a
metal level which is in each case further away from the
first gate electrode than the first or the second metal
level. The conductive connection between the first
electrode and the first gate electrode is provided by
contact holes which have been introduced into
insulation layers, are arranged above one another and
have been filled with conductive material. Arranging
the electrodes in metal levels located higher than the
first or second metal level advantageously further
reduces the thermal stressing of the storage layer. The
conductive connection between the first gate electrode
and the first electrode is advantageously provided by
contact holes which are arranged above one another and
produce a connection through a plurality of metal
levels.

The storage layer is provided in the form of an organic
layer which, for example, contains porphyrin molecules.
Such layers permanently bond charge carriers and have
predominantly low leakage currents. The gate
dielectric, through which the charge carriers can flow
out, can be made thinner. A thinner gate dielectric
offers the advantage of accelerated charging and
discharging of the storage layer. Moreover, organic
storage layers have the advantage of good scalability.
This is of great benefit to further reducing the size
of memory cells.

A memory device is provided having memory cells which
are arranged in rows, include semiconductor structures
and store a digital information item. It is preferable
for the memory cells according to the invention as

described to be arranged in the memory device. The memory device has the advantage that digital information can be stored in it in organic storage layers. On account of the permanent nature of the charge storage, leakage currents are reduced. Memory devices having the memory cells according to the invention are distinguished by permanent information storage and accelerated programming operations.

Advantageously, to provide source and drain lines, source/drain regions of memory cells which are respectively adjacent in a row are electrically conductively connected to one another by doped regions provided in the semiconductor substrate. After a predetermined number of source/drain regions which have been electrically conductively connected to one another by doped regions in the semiconductor substrate, conductive connections to interconnects, which are formed in a metal level and connect the source/drain regions of memory cells, are provided. Source and drain lines which are locally diffused with a dopant in a semiconductor substrate have the advantage of saving surface area on a semiconductor wafer for each memory cell on account of the fact that there is no need for each individual memory cell to be contact-connected to the metal level. On the other hand, lines which consist of doped semiconductor substrate have the drawback of a higher resistance. To compensate for this drawback, a conductive connection to the interconnect in the metal level is provided after a predetermined number of memory cells, for example eight or sixteen memory cells. This compensates for the drawback of an increased resistance yet nevertheless utilizes the advantage of saving surface area.

In a method for operating the claimed memory device, to program the memory device the respective storage layers of selected memory cells are charged. This is done by applying voltages to the source/drain regions contained in the selected memory cells and the second gate electrode. The storage layers are then charged by means of high-energy electrons or by means of an electron tunnelling operation through the gate dielectric. To erase the programming, the charged storage layers are discharged by means of an electron tunnelling operation to the channel region or to a source/drain region as a result of an erase voltage, which differs from the voltage applied during programming, being applied to the second gate electrode. To read the programmed memory device, the strength of a drain current is detected as a function of a charge state of the storage layer.

A voltage between the second electrode and the channel region which is high enough for at least a reduction potential suitable for the storage layer to be present at the storage layer is required to charge the storage layer in the memory cell. The required voltage can be generated by applying a positive potential to the second electrode and a negative potential to a doped region in the semiconductor substrate in which source/drain regions and channel region of a transistor are formed and which is also referred to as the well. If the voltage at the second gate electrode is sufficient to effect charging of the organic storage layer, it is advantageously also possible to apply a voltage to the drain region. If the material used for the storage layer has a plurality of redox states, it is possible to write a plurality of states by applying various voltages. Accordingly, to erase the charged storage layer, it is possible to apply the oxidation

potentials, i.e. a negative potential is applied to the second electrode and a positive potential is applied to the well.

5   To charge the storage layer in the memory cell, by way of example, a voltage of 5 V to 7 V can be applied to the drain region and a voltage of 10 V to 12 V can be applied to the second gate electrode. Under these voltage conditions, high-energy electrons are generated
10   in the channel region of the field-effect transistor, and these electrons pass through the gate dielectric into the first gate electrode and through the conductive connection to the storage layer. Electrons are received and retained by the storage layer. A
15   change in the charge state and therefore also a change in the electrical potential has occurred in the storage layer. Another way of charging the storage layer consists in utilizing an electron tunnelling operation, which is assisted by an electric field, through the
20   gate dielectric.

The electron tunnelling operation, assisted by an electric field, out of the storage layer through the gate dielectric to the channel region or to one of the
25   source/drain regions can be utilized to discharge the storage layer. By way of example, by applying a voltage of 5 V to the source region and a voltage of -8 V to the second gate electrode. To detect the charge state of the storage layer contained in the memory cell
30   during a read operation in the memory device, a defined read voltage is applied to the second gate electrode, and a voltage is applied between the source region and the drain region to generate a lateral field. The level of the drain current, above a threshold voltage, is
35   approximately linearly dependent on the level of the voltage at the second gate electrode. The drain current

is approximately absent beneath the threshold voltage.
If the storage layer is charged, for example, with
negative charge carriers and therefore has a negative
electrical potential, the threshold voltage shifts
5   toward a higher voltage at the second gate electrode.
To enable a measurable drain current to flow, a higher
voltage is applied to the second gate electrode. With a
suitable constant read voltage at the second gate
electrode, the drain current flows as a function of the
10 charge state of the storage layer; in the charged state
of the storage layer, the drain current is virtually
absent, i.e. can be allocated the logic value zero, and
in the discharged state the drain current has a finite
value and can be allocated the logic value one. A
15 detailed description of the above processes is to be
found in the book entitled Flash Memories, edited by P.
Cappelletti, C. Golla, P. Olivo, E. Zanoni, Kluwer
Academic Publishers, 53-58 (1999).

20 In the text which follows, the invention is explained
in more detail with reference to the figures, in which:

Fig. 1   shows a diagrammatic cross section through a
         memory cell corresponding to the prior art,
25
Fig. 2   shows a diagrammatic cross section through a
         first exemplary embodiment of a memory cell
         according to the invention,

30 Fig. 3   shows a diagrammatic cross section through a
         second exemplary embodiment of a memory cell
         according to the invention,

Fig. 4   shows a plan view of a diagrammatic excerpt
35   from a memory device according to the
         invention, and

Fig. 5   shows current/voltage characteristic curves of
          a field-effect transistor with organic storage
          layer.

5

Figure 1 has already been explained in more detail in
the introduction to the description.

To fabricate a memory cell 1 illustrated in Figure 2,
10   in which digital information is stored in a
      temperature-sensitive organic storage layer 10, two
      source/drain regions 5 as doped regions, which are
      spaced apart from one another by a channel region 4,
      are provided in a semiconductor substrate 17. A gate
15   dielectric 6 is arranged substantially above the
      channel region 4, and a first gate electrode 7a is
      arranged on the gate dielectric 6. The organic storage
      layer 10 is provided above the first gate electrode 7a
      between a first metal level 11a and a second metal
20   level 11b. On account of the fact that the organic
      storage layer 10 is arranged above the polycrystalline
      or monocrystalline semiconductor structures, i.e. the
      structures which are provided in the semiconductor
      substrate 17 or consist of a semiconductor substrate
25   17, it is possible for processing of the semiconductor
      structures to be concluded prior to the application of
      the organic storage layer 10. Since temperatures of up
      to 1100 degrees Celsuis are employed in the processing
      of the semiconductor structures and the organic storage
30   layer 10 is damaged at such temperatures, applying the
      organic storage layer 10 at a later time allows the
      thermal stressing of the organic storage layer 10 to be
      reduced. A conductive connection 8 connects the organic
      storage layer 10 to the first gate electrode 7a, and
35   this organic storage layer 10 can be charged by
      electrons which pass from the channel region 4 through

the gate dielectric 6 into the first gate electrode 7a.
The conductive connection is provided in the form of a
metal-filled contact hole 14 which is introduced into
an insulation layer 12. The organic storage layer 10

5   has been introduced into a hole between two metal
levels 11a, b and is arranged between a first and a
second electrode 9a, b. The second gate electrode 7b,
which is separated from the second electrode 9b by an
insulator layer 18, is located above the second

10   electrode. The second gate electrode 7b is used to
drive a field-effect transistor comprising the elements
described.

Fig. 2 reveals the elements of the field-effect

15   transistor with the organic storage layer 10 contained
in the memory cell 1. The source/drain regions 5, which
are spaced apart from one another by a channel region
4, are located in a semiconductor substrate 17. A gate
dielectric 6 is arranged above the channel region, and

20   a first gate electrode 7a is arranged on the gate
dielectric. Two metal levels 11a, b, in which the
electrodes 9a, b are marked, can be seen. The organic
storage layer 10 is located between the electrodes 9a,
b. The conductive connection 8 between the first

25   electrode 9a and the first gate electrode 7a is
illustrated in the form of a metal-filled contact hole
14 in the insulation layer 12. An insulator layer 18 is
provided on the second electrode 9b, and the second
gate electrode 7b is provided on the insulator layer.

30
To further reduce the thermal stressing on the organic
storage layer 10, it is expedient for the application
of the storage layer 10 to be shifted closer to the end
of an overall process sequence used to fabricate the

35   memory device 2. This is done, for example, by
arranging the storage layer 10 between two higher metal

levels 11 which are processed last. The conductive
connection 8 of the first electrode 9a to the first
gate electrode 7a is produced by contact holes 14,
which have been introduced into insulation layers 12,
5   have been stacked on top of one another, have been
filled with metal and allow contact through metal
levels 11 below.

The exemplary embodiment of the memory cell 1 shown in
10   Fig. 3 differs from the exemplary embodiment of the
memory cell 1 illustrated in Fig. 2 by virtue of the
form of its conductive connection 8. The organic layer
10 is located between two higher metal levels 11. The
conductive connection 8 comprises contact holes 14
15   which are stacked on top of one another, have been
filled with metal, have been introduced into the
insulation layers 12 provided between the metal levels
11 and produce contact through a plurality of metal
levels 11 which include interconnects 13 and contact
20   holes 14.

To fabricate a memory device 2 from the memory cells 1,
the memory cells 1 are, for example, arranged in rows
and columns. Memory cells 1 which are in each case
25   adjacent in rows and columns are connected to one
another by interconnects 13 which are arranged
perpendicular to one another and lie above one another
at crossing points 15. One interconnect 13 connects
source/drain regions 5 of memory cells 1 which are
30   adjacent in a row and is also referred to as a bit line
13b. The other interconnect 13 connects the second gate
electrodes 7b of the memory cells 1 which are adjacent
in the columns and is also referred to as an addressing
line 13a. Both bit line 13b and addressing line 13a are
35   in each case formed in a respective metal level 11.
Since the bit line 13b is supposed to make contact with

the respective source/drain region 5 in each memory cell 1, and contacts would take up space in the memory cell 1, to save on surface area, the source/drain regions 5 of the memory cells 1 are electrically
5   conductively connected to one another by doped regions 16 in the semiconductor substrate 17. A conductive connection 8 to the bit line 13b is only provided every 8 or 16 memory cells 1, for example.

10   An excerpt from the memory device 2 can be seen in Figure 4. This figure illustrates bit lines 13b and addressing lines 13a arranged in a crossed pattern. The memory cells 1 arranged in rows and columns are located at the crossing points 15. The doped regions 16, which
15   are formed as lines and connect the source/drain regions 5 of memory cells 1 that are adjacent in a row to one another, can be seen in the excerpt, as can the conductive connection 8 to the bit line 13b.

20   The current/voltage characteristic curves of a memory cell 1 with organic storage layer 10 illustrated in Figure 5 have already been explained in more detail in the introduction to the description.

List of Designations

	1	Memory cell
	2	Memory device
5	4	Channel region
	5	Source/drain region
	6	Gate dielectric
	7a	First gate electrode
	7b	Second gate electrode
10	8	Conductive connection
	9a	First electrode
	9b	Second electrode
	10	Storage layer
	11	Metal level
15	11a	First metal level
	11b	Second metal level
	12	Insulation layer
	13	Interconnect
	13a	Addressing line
20	13b	Bit line
	14	Contact hole
	15	Crossing points
	16	Doped region
	17	Semiconductor substrate
25	18	Insulator layer